

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A multiply-accumulate module comprising:
2 a multiply-accumulate core, wherein said multiply-accumulate
3 core comprises:

4 a plurality of Booth encoder cells;

5 a plurality of Booth decoder cells connected to at least
6 one of said Booth encoder cells, said plurality of Booth decoder
7 cells including at least one first Booth decoder cell and at least
8 one second Booth decoder cell, said at least one first Booth
9 decoder cell structurally the same as said at least one second
10 Booth decoder cells; and

11 a plurality of Wallace tree cells connected to at least
12 one of said Booth decoder cells, said plurality of Wallace tree
13 cells including at least one first Wallace tree cell and at least
14 one second Wallace tree cell, said at least one first Wallace tree
15 cell structurally the same as said at least one second Wallace tree
16 cell;

17 wherein said multiply-accumulate module includes at least one
18 critical path, a said at least one critical path being an
19 electrical path for which an amount of time that it takes for an
20 electrical signal to travel from an input of said multiply-
21 accumulate core to an output of said multiply-accumulate core is
22 greater than or equal to a predetermined amount of time and less
23 than a longest amount of time that it takes any other electrical
24 signal to travel from said input of said multiply-accumulate core
25 to said output of said multiply-accumulate core, wherein said
26 predetermined amount of time is less than a said longest amount of
27 time that it takes any other electrical signal to travel from said

28 ~~input of said multiply accumulate core to said output of said~~
29 ~~multiply accumulate core;~~

30 wherein said at least one first Wallace tree cell or said at
31 least one first Booth decoder cell are disposed on said at least
32 one critical path;

33 wherein said at least one second Wallace tree cell and said at
34 least one second Booth decoder cell are not disposed on any of said
35 at least one critical path;

36 wherein said at least one first Wallace tree cell or said at
37 least one first Booth decoder cell comprises a first plurality of
38 transistors, and at least one second Wallace tree cell or at least
39 one second Booth decoder cell comprises a second plurality of
40 transistors; and

41 a width of at least one of said first plurality of transistors
42 is greater than a width of a corresponding one of said second
43 plurality of transistors.

2. (Canceled)

1 3. (Previously Presented) The multiply-accumulate module of claim
2 1, wherein said multiply-accumulate core further comprises:

3 an adder connected to at least one of said Wallace tree cells;

4 a saturation detector connected to said adder, wherein said
5 multiply-accumulate module further comprises:

6 at least one input register connected to at least one of said
7 Booth encoding cells; and

8 at least one result register connected to said saturation
9 detector.

4 to 8. (Canceled)

1 9. (Original) The multiply-accumulate module of claim 1, wherein
2 said at least one second cell is a most significant bit or a least
3 significant bit and said at least one first cell is not a most
4 significant bit or a least significant bit.

1 10. (Currently Amended) A parallel multiplier comprising:
2 a parallel multiplier core, wherein said parallel multiplier
3 core comprises:

4 a plurality of Booth encoder cells;
5 a plurality of Booth decoder cells connected to at least
6 one of said Booth encoder cells, said plurality of Booth decoder
7 cells including at least one first Booth decoder cell and at least
8 one second Booth decoder cell, said at least one first Booth
9 decoder cell structurally the same as said at least one second
10 Booth decoder cells; and

11 a plurality of Wallace tree cells connected to at least
12 one of said Booth decoder cells, said plurality of Wallace tree
13 cells including at least one first Wallace tree cell and at least
14 one second Wallace tree cell, said at least one first Wallace tree
15 cell structurally the same as said at least one second Wallace tree
16 cell;

17 wherein said multiply-accumulate module includes at least one
18 critical path, a said at least one critical path being an
19 electrical path for which an amount of time that it takes for an
20 electrical signal to travel from an input of said multiply-
21 accumulate core to an output of said multiply-accumulate core is
22 greater than or equal to a predetermined amount of time and less
23 than a longest amount of time that it takes any other electrical
24 signal to travel from said input of said multiply-accumulate core
25 to said output of said multiply-accumulate core, wherein said
26 predetermined amount of time is less than a said longest amount of
27 time ~~that it takes any other electrical signal to travel from said~~

28 ~~input of said multiply accumulate core to said output of said~~
29 ~~multiply accumulate core;~~

30 wherein said at least one first Wallace tree cell or said at
31 least one first Booth decoder cell are disposed on said at least
32 one critical path;

33 wherein said at least one second Wallace tree cell and said at
34 least one second Booth decoder cell are not disposed on any of said
35 at least one critical path;

36 wherein said at least one first Wallace tree cell or said at
37 least one first Booth decoder cell comprises a first plurality of
38 transistors, and at least one second Wallace tree cell or at least
39 one second Booth decoder cell comprises a second plurality of
40 transistors; and

41 a width of at least one of said first plurality of transistors
42 is greater than a width of a corresponding one of said second
43 plurality of transistors.

11. (Canceled)

1 12. (Previously Presented) The parallel multiplier of claim 10,
2 wherein said parallel multiplier core further comprises:

3 an adder connected to at least one of said Wallace tree cells;
4 a saturation detector connected to said adder, wherein said
5 parallel multiplier further comprises:

6 at least one input register connected to at least one of said
7 Booth encoding cells; and

8 at least one result register connected to said saturation
9 detector and at least one of said Wallace tree cells.

13 to 17. (Canceled)

1 18. (Original) The multiply-accumulate module of claim 10, wherein
2 at least one second cell is a most significant bit or a least
3 significant bit and at least one first cell is not a most
4 significant bit or a least significant bit.

1 19. (Currently Amended) A method of designing a multiply-
2 accumulate module comprising the steps of:

3 providing a multiply-accumulate core, wherein the step of
4 providing a multiply-accumulate core comprises the steps of:

5 providing a plurality of Booth encoder cells;

6 connecting a plurality of Booth decoder cells to at least
7 one of said Booth encoder cells;

8 connecting a plurality of Wallace tree cells to at least
9 one of said Booth decoder cells;

10 defining at least one critical path ~~wherein within~~ said
11 multiply-accumulate module, a said at least one critical path being
12 an electrical path for which an amount of time that it takes for an
13 electrical signal to travel from an input of said multiply-
14 accumulate core to an output of said multiply-accumulate core is
15 greater than or equal to a predetermined amount of time and less
16 than a longest amount of time that it takes any other electrical
17 signal to travel from said input of said multiply-accumulate core
18 to said output of said multiply-accumulate core, wherein said
19 predetermined amount of time is less than a said longest amount of
20 time ~~that it takes any other electrical signal to travel from said~~
21 ~~input of said multiply accumulate core to said output of said~~
22 ~~multiply accumulate core~~;

23 defining a Wallace tree cell disposed on said at least
24 one critical path as a first Wallace tree cell;

25 defining a Wallace tree cell not disposed on any of said
26 at least one critical path as second Wallace tree cell;

27 defining a Booth decoder cell disposed on said at least
28 one critical path as a first Booth decoder cell;
29 defining a Booth decoder cell not disposed on any of said
30 at least one critical path as second Booth decoder cell;
31 constructing each first Wallace tree cell and each first
32 Booth decoder cell of a first plurality of transistors, each first
33 Wallace tree cell structurally the same as each second Wallace tree
34 cell, and constructing each second Wallace tree cell and each
35 second Booth decoder cell of a second plurality of transistors,
36 each first Booth decoder cell structurally the same as each second
37 Booth decoder cell;
38 selecting a first width for at least one of said first
39 plurality of transistors; and
40 selecting a second width for at least one of said second
41 plurality of transistors which is less than said first width of a
42 corresponding one of said first plurality of transistors.

1 20. (Currently Amended) A method of designing a parallel
2 multiplier comprising the steps of:
3 providing a parallel multiplier core, wherein the step of
4 providing a parallel multiplier core comprises the steps of:
5 providing a plurality of Booth encoder cells;
6 connecting a plurality of Booth decoder cells to at least
7 one of said Booth encoder cells;
8 connecting a plurality of Wallace tree cells to at least
9 one of said Booth decoder cells;
10 defining at least one critical path ~~wherein~~ within said
11 multiply-accumulate module, a said at least one critical path being
12 an electrical path for which an amount of time that it takes for an
13 electrical signal to travel from an input of said multiply-
14 accumulate core to an output of said multiply-accumulate core is
15 greater than or equal to a predetermined amount of time and less

16 than a longest amount of time that it takes any other electrical
17 signal to travel from said input of said multiply-accumulate core
18 to said output of said multiply-accumulate core, wherein said
19 predetermined amount of time is less than a said longest amount of
20 time that it takes any other electrical signal to travel from said
21 input of said multiply accumulate core to said output of said
22 multiply accumulate core;

23 defining a Wallace tree cell disposed on said at least
24 one critical path as a first Wallace tree cell;

25 defining a Wallace tree cell not disposed on any of said
26 at least one critical path as second Wallace tree cell;

27 defining a Booth decoder cell disposed on said at least
28 one critical path as a first Booth decoder cell;

29 defining a Booth decoder cell not disposed on any of said
30 at least one critical path as second Booth decoder cell;

31 constructing each first Wallace tree cell and each first
32 Booth decoder cell of a first plurality of transistors, each first
33 Wallace tree cell structurally the same as each second Wallace tree
34 cell, and constructing each second Wallace tree cell and each
35 second Booth decoder cell of a second plurality of transistors,
36 each first Booth decoder cell structurally the same as each second
37 Booth decoder cell;

38 selecting a first width for at least one of said first
39 plurality of transistors; and

40 selecting a second width for at least one of said second
41 plurality of transistors which is less than said first width of a
42 corresponding one of said first plurality of transistors.